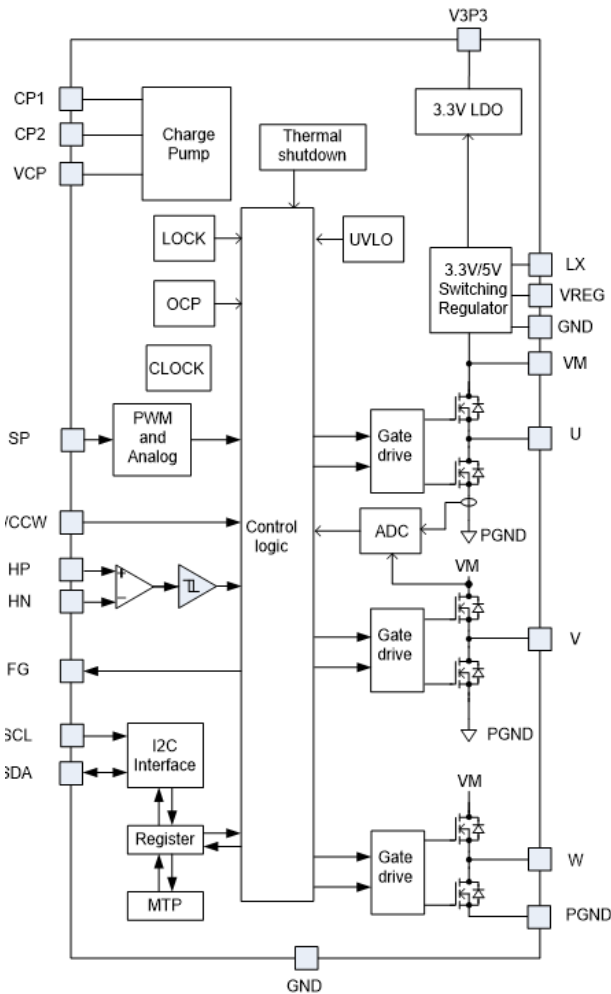




SY21604

3-ph BLDC Sinewave Driver

With integrated low RDS(on) MOSFETS



Power Supply Range 5V to 40V

Three Half H-Bridge drivers with 2Arms(3Apk)

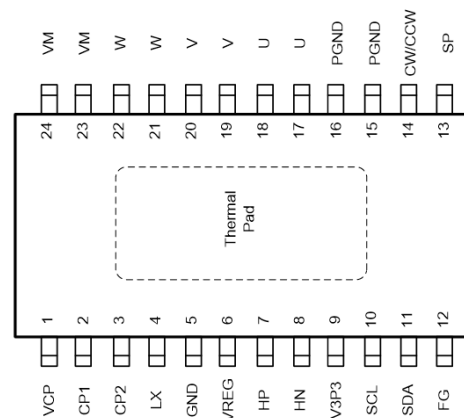
Sensor-less or Single Hall Sensor control

Integrated 180° SPWM control algorithm

I²C interface for configuration and control

Speed control via SP pin (PWM/Analog) or I²C

TSSOP24E package (Thermally enhanced package)



The SY21604 is a fully integrated driver for sensorless control of 3-ph Brushless DC (BLDC) motors using a 180° sinewave modified PWM (SPWM) signal. Support for a single Hall Effect Sensor is also possible if required by the application.

Extensive protection mechanisms are implemented for Over Current, Short Circuit, UVLO and Over Temperature, including abnormal motor state. The device is configured and controlled via I²C and provides speed setting using the SP pin (PWM, Analog) or I²C.

Robust - Highly Integrated - Cost saving

Silergy's 3-ph BLDC Drivers simplify the Art of Motor control



SY21604

3-ph BLDC Sinewave Driver

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The SY21604 has a number of significant technical enhancements as described below.

FEATURE	SY21604	Notes
Supply Voltage AbsMax (V)	-0.3 ~ +40	A higher voltage specification allows for a more robust design which is better suited to industrial environments
Supply Voltage operational (V)	+5 ~ +32	
Program Voltage (V)	+5 ~ +40	
Open Loop Current (A)	2.4	Supports a larger traction force during startup
EEPROM (bits)	144	Larger NV storage for Motor Parameters
Motor Parameter Changes	More Robust	Silergy's patented control algorithm is more robust to parameter changes
SP pin voltage (V)	3.3 or 5	Dual voltage PWM speed control for flexibility
MOSFET RDS(on) (Ω)	230	Lower RDS(on) improves temperature performance
Hall Sensor Inputs	1	Supports Single Hall Sensor BEMF detection (if required)

A standard Evaluation Board is available, as shown in FIG 1. There is also a more complete reference design with isolated ACDC Flyback stage providing 26Vdc, from a universal 230Vac mains source, as shown in FIG 2.

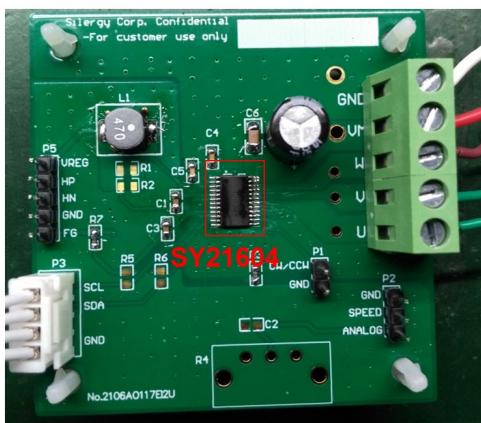


FIG 1. SY21604 EVB

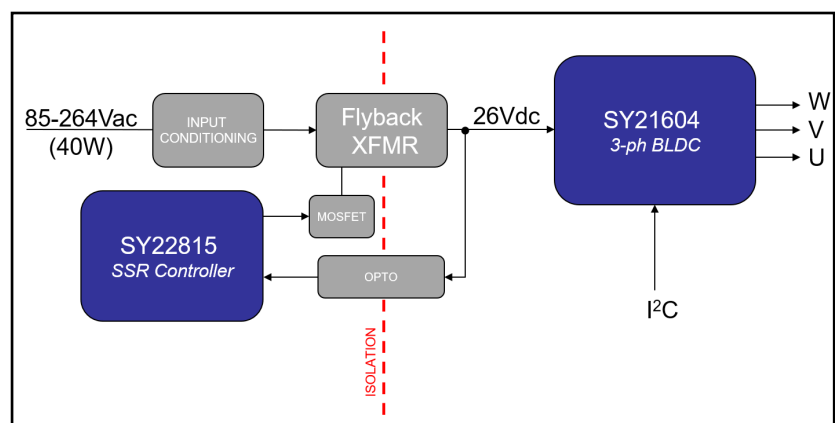


FIG 2. SY21604 Ref Design with ACDC stage

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