

JULY 2005

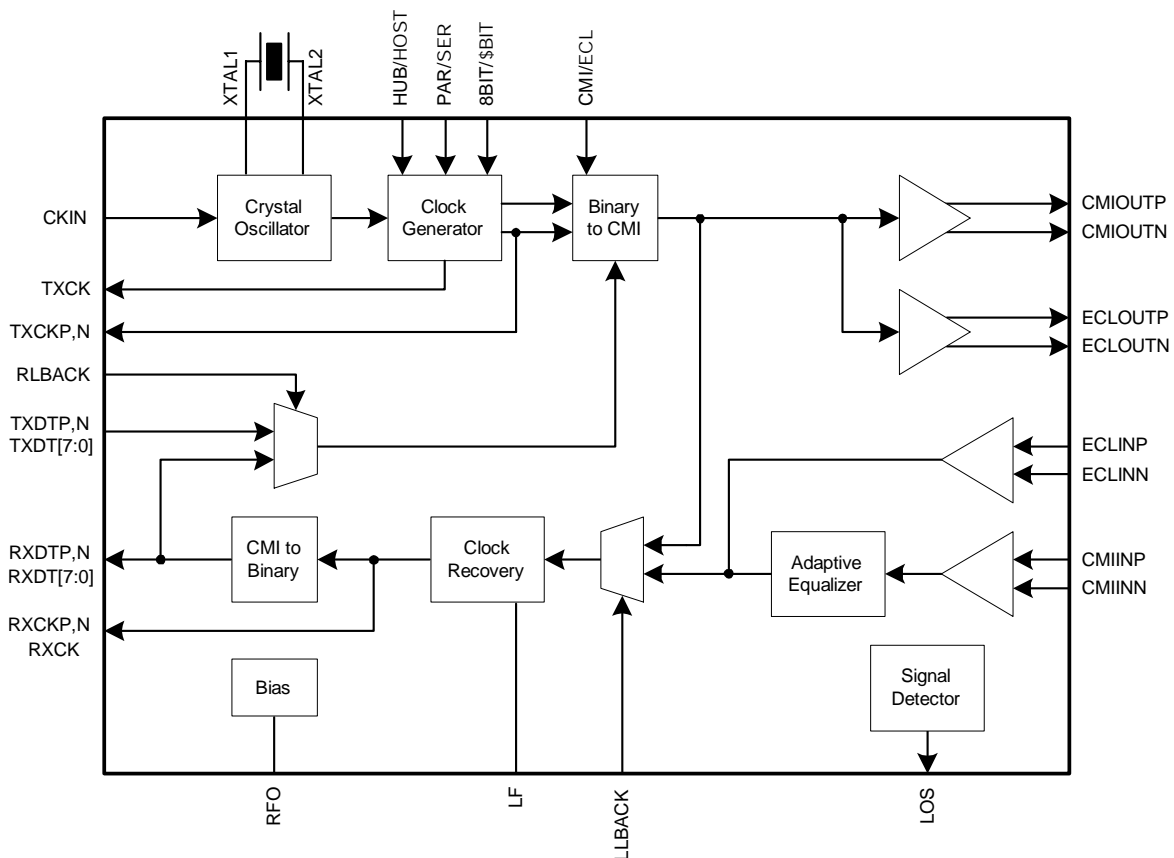
DESCRIPTION

The 78P2253 is a transceiver IC designed for 155.52Mbit/s (OC-3 or STM-1e) transmission. It is used at the interface to a 75Ω coaxial cable using CMI coding or a fiber optic module using NRZ coding. Interface to digital framer circuits is accomplished via a serial PECL or parallel CMOS interface.

The transmitter includes a PLL to multiply the reference clock to the transmission frequency. The receiver provides adaptive equalization for accurate clock and data recovery. The 78P2253 is built in a BiCMOS technology for high performance and low power operation. It operates with a 3.3V or 5V power supply and is packaged in a 64-pin TQFP.

FEATURES

- Analog interface for CMI coded, STM-1e transmission using 75Ω coaxial cable
- PECL Interface for connection to Fiber Optic Modules for SONET OC3 applications
- Compliant with ITU-T G.703, G.825, G.958; Telcordia TR-NWT-00253; and ANSI T1.105.03-1994, T1.105.05-1994, T1.102-1993
- Integrated Clock Recovery Unit (CRU)
- Serial PECL system interface
- 4/8 bit Parallel CMOS system interfaces
- Adaptive Equalization
- Integrated Clock Multiplier PLL
- Advanced BiCMOS Process
- Single 3.3V or 5V power supply

BLOCK DIAGRAM


FUNCTIONAL DESCRIPTION

The 78P2253 contains all the necessary transmit and receive circuitry for connection between 155.52Mbit/s signals and digital Framers ICs.

DIGITAL INTERFACE

The digital interface of the 78P2252 can operate as a Serial PECL, 4-bit Parallel CMOS, or 8-bit Parallel CMOS interface. These modes are controlled by the PAR/SER and 8BIT/\$BIT pins as shown in the following table.

| Mode | PAR SER | 8BIT \$BIT | Data pins | Clock pins | Clock Frequency |
|-------------------|------------|---------------|------------------------|--------------------|--------------------|
| Serial | 0 | X | TXDTP,N RXDTP,N | TXCKP,N RXCKP,N | 155.52 MHz |
| 4-bit Parallel | 1 | 0 | TXDT[3:0] RXDT[3:0] | TXCK RXCK | 38.88 MHz |
| 8-bit Parallel | 1 | 1 | TXDT[7:0] RXDT[7:0] | TXCK RXCK | 19.44 MHz |

NETWORK INTERFACE MEDIUM CHOICES

When the CMI/ECL pin is high, the chip is in CMI mode and connects to 75Ω coaxial cable for STM-1e interfaces. In this mode, the CMIOUTP and CMIOUTN pins are active and connect the chip to the coaxial cable through a transformer and matching resistors. In CMI mode the transmitter shapes the transmit pulses to meet the appropriate template and the adaptive equalizer corrects the received signal for dispersive attenuation. In CMI mode the NRZ data signal from the digital Framer IC is converted to CMI code by the Binary to CMI encoder. The ECLOUTP and ECLOUTN pins are inoperative and should be left open.

When the CMI/ECL pin is low, the chip is in ECL mode and connects to a fiber optics module for OC-3 interfaces. The output data signal from the pins ECLOUTP and ECLOUTN have PECL levels. In this mode, the CMI pins are inoperative and should be left open. The CMI encoder/decoder is disabled.

TRANSMITTER OPERATION

The transmitter section generates an analog signal for transmission through either a fiber optic module or a transformer onto the coaxial cable.

When the chip is in serial mode (PAR/SER low), serial NRZ data is input from the digital Framer IC to the 78P2253 on the TXDTP and TXDTN pins at PECL levels. The data is timed with the clock generated by the 78P2253 on the TXCKP,N pins. In this mode the 8BIT/\$BIT control pin is ignored.

When the chip is in parallel mode (PAR/SER high), parallel data is input from the digital Framer IC to the 78P2253 on the TXDT[7:0] pins. The input data is timed with the transmit clock output from the TXCK pin. When 8BIT/\$BIT is high, all eight bits of TXDT[7:0] are used and the clock frequency at TXCK is one-eighth the standard frequency. When 8BIT/\$BIT is low, the lower four bits TXDT[3:0] are used and TXCK is one-fourth the standard frequency.

Note that the first bit output from the ECL/CMI interface (CMIOUTP,N for CMI mode and ECLOUTP,N for ECL mode) is the most significant bit on the parallel interface, TXDT7 in eight-bit mode, TXDT3 in four-bit mode.

RECEIVER OPERATION

The receiver accepts serial, CMI coded data, at 155.52Mbit/s from the CMI inputs or NRZ coded data from the ECL inputs. In both cases, the clock signal is recovered using a low jitter PLL circuit.

In CMI mode, the inputs CMIINP and CMIINN receive the input signal from a coaxial cable that is transformer-coupled to the chip. The received signal is equalized for dispersive cable attenuation and decoded in the CMI to binary decoder. In CMI mode, the ECL pins should be left open.

In ECL mode, the pins ECLINP and ECLINN receive the input signal from a fiber module.

In serial mode, the received data is output on the RXDTP and RXDTN pins and the recovered clock is output on the RXCKP and RXCKN pins.

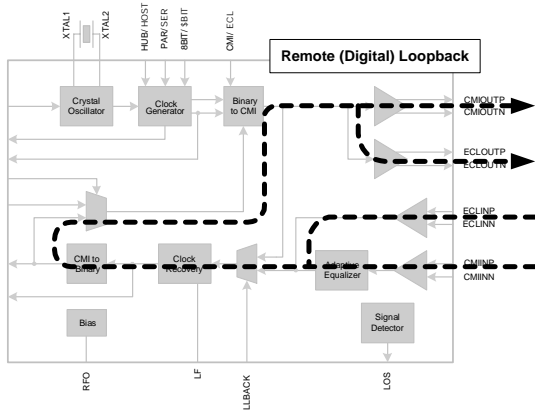
In parallel mode, the received data is converted to parallel, eight bits if 8BIT/\$BIT is high and four if it is low. The first bit received will arrive on the most significant output pin, RXDT[7] in eight-bit mode and RXDT[3] in four bit mode. The recovered clock is output on the RXCK pin.

The LOS pin goes high when the signal detector detects a loss-of-signal condition according to G.775 specifications.

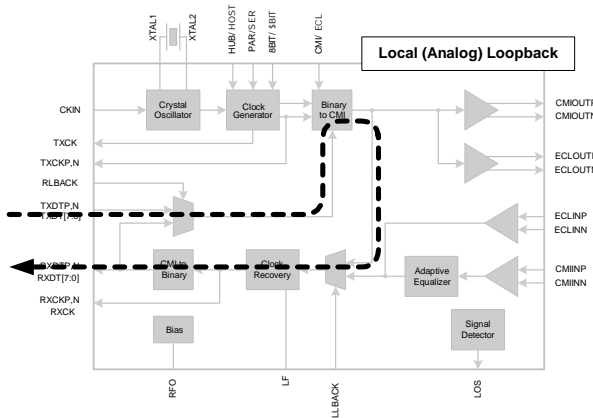
LOOPBACK OPERATION

Remote and Local Loopback modes in the 78P2252 are controlled by the RLBACK and LLBACK pins respectively.

When in Remote (Digital) Loopback mode (RLBACK logic high), the received data is internally routed onto the transmitter inputs. Note that any input data on the TXDTP,N pins or TXDT[7:0] pins is ignored in remote loopback mode.



When in Local (Analog) Loopback mode (LLBACK logic high), the transmit output signals are internally routed to the receiver inputs. Note that Local Loopback mode is disabled when HUB/HOST is low or RLBACK is high.



REFERENCE CLOCK

The HUB/HOST pin selects the source of the reference signal used for the internal transmit clock generator.

In Hub mode (HUB/HOST logic high), the transmit clock reference is derived from either a crystal oscillator applied to the XTAL1 and XTAL2 pins or a reference clock input applied at the CKIN pin. The reference frequency should be one-eighth the line rate frequency at 19.44MHz and should be applied in one of the following configurations.

Hub Mode Configurations

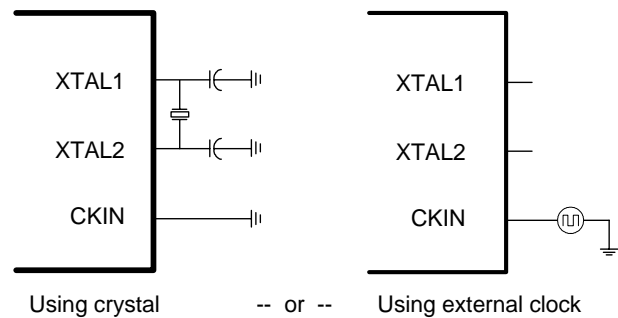


Figure 1

In Host mode (HUB/HOST logic low), the transmit clock reference is derived from the recovered receive clock. Note that the recovered receive clock is also used as the reference clock when Remote Loopback is enabled.

| .LBACK | RLBACK | HUB/HOST | reference Clock |
|--------|--------|----------|--------------------|
| 0 | 0 | 1 | CKIN or XTAL1,2 |
| 1 | 0 | 1 | CKIN or XTAL1,2 |
| X | 1 | 1 | Recovered Rx Clock |
| X | X | 0 | Recovered Rx Clock |

PIN DESCRIPTION
LEGEND

| TYPE | DESCRIPTION | TYPE | DESCRIPTION |
|------|---------------------|------|---------------------|
| A | Analog Pin | PI | PECL Digital Input |
| CI | CMOS Digital Input | PO | PECL Digital Output |
| CO | CMOS Digital Output | S | Supply Pin |

TRANSMIT PINS

| NAME | PIN | TYPE | DESCRIPTION |
|--------------------|----------|------|---|
| TXDTP TXDTN | 19 20 | PI | Transmit Data Inputs - Serial Mode. |
| TXCKP TXCKN | 22 23 | PO | Transmit Clock Output - Serial Mode. |
| TXDT[7:0] | 11-18 | CI | Transmit Data Inputs – Parallel Mode. TXDT[7:4] are ignored in 4-bit mode. |
| TXCK | 10 | CO | Reference Clock Output – Serial mode. Transmit Clock Output – Parallel Mode. |
| CMIOUTP CMIOUTN | 60 59 | A | Transmit Output in CMI mode. No signal is output in ECL mode. |
| ECLOUTP ECLOUTN | 56 55 | PO | Transmit Outputs for ECL mode. No signal is output in CMI mode. |

RECEIVE PINS

| NAME | PIN | TYPE | DESCRIPTION |
|------------------|----------|------|--|
| CMIINP CMIINN | 50 49 | A | Receive inputs in CMI mode. Transformer coupled from the coaxial cable. Ignored in ECL mode. |
| ECLINP ECLINN | 52 51 | PI | Receiver inputs in ECL mode. Ignored in CMI mode. |
| RXCKP RXCKN | 25 26 | PO | Recovered Receive Clock – Serial Mode. |
| RXCK | 38 | CO | Recovered Receive Clock – Parallel Mode. |
| RXDTP RXDTN | 27 28 | PO | Receive data – Serial Mode. |
| RXDT[7:0] | 30-37 | CO | Receive data – Parallel Mode. In 4-bit mode RXDT[3:0] are used and RXDT[7:4] are pulled low. |

PIN DESCRIPTION (continued)

REFERENCE CLOCK PINS

| NAME | PIN | TYPE | DESCRIPTION |
|-------|-----|------|--|
| XTAL1 | 5 | A | Crystal Pins. Connect as in Figure 1. |
| XTAL2 | 6 | | |
| CKIN | 9 | CI | Reference clock input. The crystal oscillator connections should be left open when used. Connect as in Figure 1. |

CONTROL AND STATUS PINS

| NAME | PIN | TYPE | DESCRIPTION |
|------------|-----|------|--|
| RLBACK | 41 | CI | Loopback receiver output to transmitter input. |
| LLBACK | 42 | CI | Loopback transmitter output to receiver input. Disabled when HUB/HOST is low or RLBACK is high. |
| HUB/HOST | 2 | CI | In HUB mode (input high) the transmit reference clock is derived from the CKIN pin or the crystal oscillator. In HOST mode (input low) the transmit reference clock is derived from the recovered receive clock. |
| CMI/ECL | 1 | CI | Selects CMI (input high) or ECL (input low) modes. |
| 8BIT/\$BIT | 63 | CI | Selects 8 bit parallel data when high and 4-bit parallel mode when low. In serial mode this pin is ignored. |
| PAR/SER | 62 | CI | Selects parallel mode when high and serial mode when low. |
| LOS | 39 | CO | High during a loss-of-signal condition. |

ANALOG PINS

| NAME | PIN | TYPE | DESCRIPTION |
|------|-----|------|------------------------------|
| RFO | 46 | A | External reference resistor. |
| LF | 44 | A | PLL loop filter capacitor. |

POWER SUPPLY PINS

It is recommended that all VCC pins be connected to a single power supply plane and all GND pins be connected to a single ground plane.

| NAME | PIN | TYPE | DESCRIPTION |
|------|--|------|---------------|
| VCC | 3, 8, 24, 40, 43, 53, 54, 57 | S | Power Supply. |
| GND | 4, 7, 21, 29, 45, 47, 48, 58, 61, 64 | S | Ground. |

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond these limits may permanently damage the device.

| PARAMETER | RATING |
|---------------------|------------------------------------|
| Supply Voltage | 7 VDC |
| Storage Temperature | -65 to 150° C |
| Pin Voltage | -0.3 to (V _{CC} +0.3) VDC |
| Pin Current | ±100 mA |

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted all specifications are valid over these temperatures and supply voltage ranges.

| PARAMETER | RATING |
|-------------------------------|----------------------------|
| DC Voltage Supply, VCC | 3.3 ± 0.3 VDC; 5 ± 0.5 VDC |
| Ambient Operating Temperature | -40 to 85°C |

DC CHARACTERISTICS:

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------------------------|-----------------|------------------------|-----|-----|-----|------|
| Supply Current (Parallel Mode) | I _{CC} | V _{CC} = 3.3V | | 140 | 165 | mA |
| | | V _{CC} = 5.0V | | 150 | 175 | |
| Supply Current (Serial Mode) | I _{CC} | V _{CC} = 3.3V | | 210 | 245 | mA |
| | | V _{CC} = 5.0V | | 280 | 330 | |

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL INPUT CHARACTERISTICS
Pins of type CI

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------------|----------|------------|-------------|-----|-------------|------|
| Input Voltage Low | Vil | | | | Vcc/2 - 0.9 | V |
| Input Voltage High | Vih | | Vcc/2 + 0.9 | | | V |
| Input Current | Iil, Iih | | -10 | | 10 | μA |
| Input Capacitance | Cin | | | 10 | | pF |

Pins of type PI

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------------|--------|-----------------|------|-----|------|------|
| Input Voltage Low | Vil | Relative to Vcc | | | -1.5 | V |
| Input Voltage High | Vih | Relative to Vcc | -1.1 | | | V |

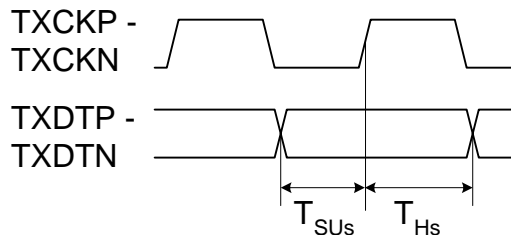
DIGITAL OUTPUT CHARACTERISTICS
Pins of type CO

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|--------|------------|-----|-----|-----|------|
| Output Voltage Low | Vol | | | 0.6 | 0.7 | V |
| Output Voltage High | Voh | Below Vcc | | 0.6 | 0.7 | V |
| Transition Time | Tt | | | 3.5 | | ns |

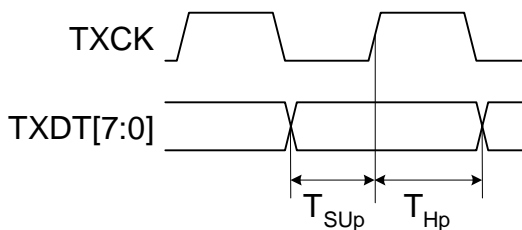
Pins of type PO

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|--------|---|------|------|------|------|
| Output Voltage Low | Vol | Vcc Reference biased at Vcc -1.5V with 50 ohm | -1.7 | -1.4 | -1.3 | V |
| Output Voltage High | Voh | Vcc Reference biased at Vcc -1.5V with 50 ohm | -1.1 | -0.9 | -0.7 | V |
| Rise Time | Tr | | | 1 | 3 | ns |
| Fall Time | Tf | | | 1 | 3 | ns |

ELECTRICAL SPECIFICATIONS (continued)

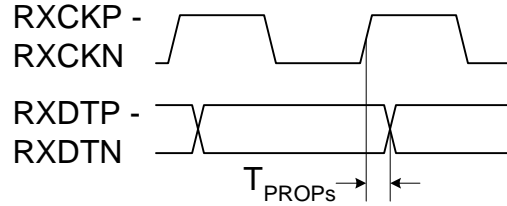
DIGITAL TIMING CHARACTERISTICS
Transmit Interface


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|-----------|-------------|-----|-----|-----|------|
| Transmit Setup Time | T_{SUs} | Serial Mode | 1.5 | | | ns |
| Transmit Hold Time | T_{Hs} | Serial Mode | 1.5 | | | ns |
| TXCKP,N Duty Cycle | | | 40 | | 60 | % |

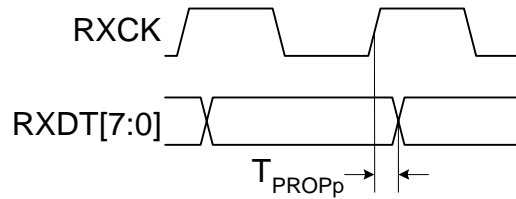


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------|-----------|---------------|-----|-----|-----|------|
| Transmit Setup Time | T_{SUp} | Parallel Mode | 3.5 | | | ns |
| Transmit Hold Time | T_{Hp} | Parallel Mode | 2.5 | | | ns |
| TXCK Duty Cycle | | | 40 | | 60 | % |

ELECTRICAL SPECIFICATIONS (continued)

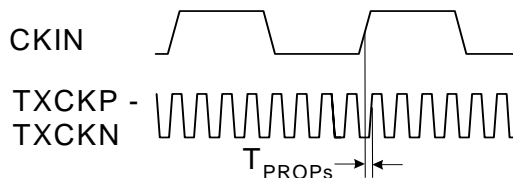
DIGITAL TIMING CHARACTERISTICS
Receive Interface


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------------|-------------|-------------|-----|-----|-----|------|
| Receive Propagation Delay | T_{PROPS} | Serial Mode | | 2.4 | 3.0 | ns |
| RXCKP,N Duty Cycle | | | 40 | | 60 | % |

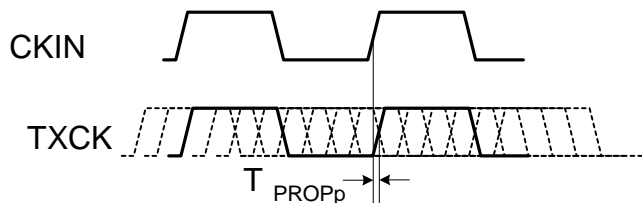


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---------------------------|-------------|---------------|-----|-----|-----|------|
| Receive Propagation Delay | T_{PROPP} | Parallel Mode | | 4.0 | | ns |
| RXCKP,N Duty Cycle | | | 40 | | 60 | % |

ELECTRICAL SPECIFICATIONS (continued)

DIGITAL TIMING CHARACTERISTICS
Reference Clock Interface


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|-----------------------|-------------|-------------|-----|-----|-----|------|
| CKIN to TXCKP/N Delay | T_{PROPs} | Serial Mode | 3.1 | 4.6 | 5.6 | ns |

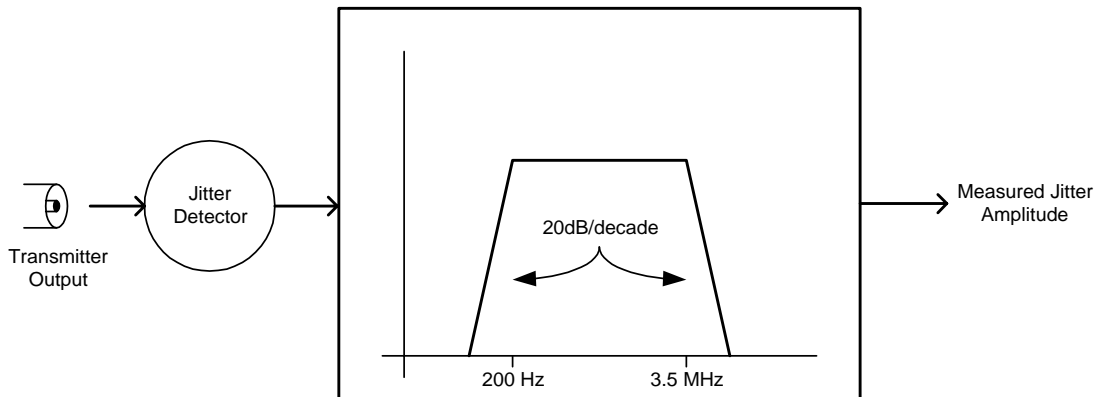


| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|------------------------------------|-------------|---------------------|-----|-----|-----|------|
| CKIN to closes phase of TXCK delay | T_{PROPs} | Parallel 8 bit Mode | 1.6 | 3.7 | 5.7 | ns |

ELECTRICAL SPECIFICATIONS (continued)

TRANSMITTER OUTPUT JITTER

The transmit jitter specification ensures compliance with ITU-T G.825, G.958 and ANSI T1.105.03-1994 for STM-1, STS-3, and OC-3 rates. The corner frequency of the transmit PLL is nominally 3.0 MHz.



| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---------------------------|-------------------|-----|-----|-------|------|
| Transmitter Output Jitter | 200 Hz to 3.5 MHz | | | 0.075 | UI |

TRANSMITTER SPECIFICATIONS FOR CMI INTERFACE IN STM-1E MODE

Bit Rate: 155.52Mbit/s \pm 20ppm

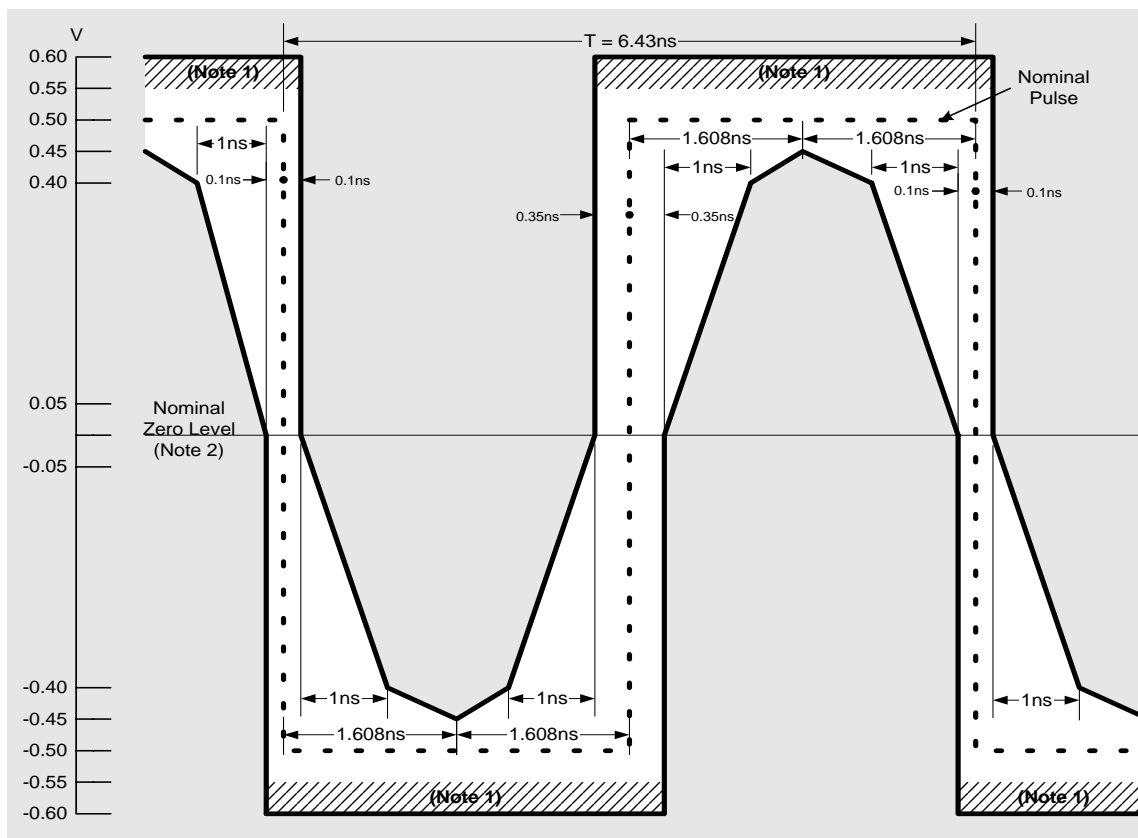
Code: coded mark inversion (CMI)

The following specifications are met with the external components for STM-1 operation configured with a recommended 1:1 transformer. With the coaxial output port driving a 75 Ω load, the output pulses conform to the templates in Figure 2 and Figure 3.

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|-----------------------------|---|-------|-----|------|------|
| Peak-to-peak Output Voltage | Template | 0.9 | | 1.1 | V |
| Rise/ Fall Time | 10-90% | | | 2 | ns |
| Transition Timing Tolerance | Negative Transitions | -0.1 | | 0.1 | ns |
| | Positive Transitions at Interval Boundaries | -0.5 | | 0.5 | ns |
| | Positive Transitions at mid-interval | -0.35 | | 0.35 | ns |

TRANSMISSION PERFORMANCE

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|-------------|----------------|-----|-----|-----|------|
| Return Loss | 7MHz to 240MHz | 15 | | | dB |

ELECTRICAL SPECIFICATIONS (continued)


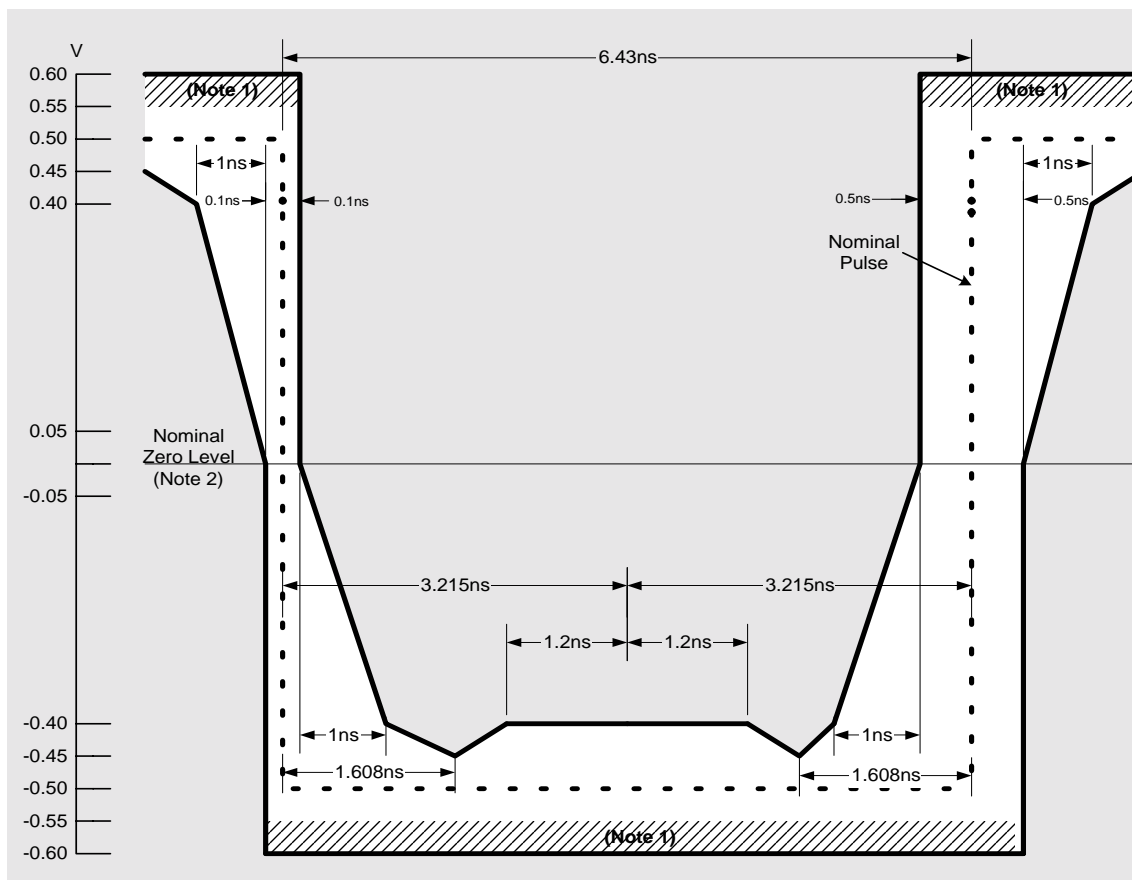
Note 1 – The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF , to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed $\pm 0.05\text{V}$. This may be checked by removing the input signal again and verifying that the trace lies with $\pm 0.05\text{V}$ of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between -0.4V and 0.4V , and should not exceed 2ns.

Figure 2 – Mask of a Pulse corresponding to a binary Zero in STS-3 mode.



Note 1 – The maximum “steady state” amplitude should not exceed the 0.55V limit. Overshoots and other transients are permitted to fall into the shaded area bounded by the amplitude levels 0.55V and 0.6V, provided that they do not exceed the steady state level by more than 0.05V.

Note 2 – For all measurements using these masks, the signal should be AC coupled, using a capacitor of not less than 0.01 μF , to the input of the oscilloscope used for measurements. The nominal zero level for both masks should be aligned with the oscilloscope trace with no input signal. With the signal then applied, the vertical position of the trace can be adjusted with the objective of meeting the limits of the masks. Any such adjustment should be the same for both masks and should not exceed $\pm 0.05\text{V}$. This may be checked by removing the input signal again and verifying that the trace lies with $\pm 0.05\text{V}$ of the nominal zero level of the masks.

Note 3 – Each pulse in a coded pulse sequence should meet the limits of the relevant mask, irrespective of the state of the preceding or succeeding pulses, with both pulse masks fixed in the same relation to a common timing reference, i.e. with their nominal start and finish edges coincident. The masks allow for HF jitter caused by intersymbol interference in the output stage, but not for jitter present in the timing signal associated with the source of the interface signal. When using an oscilloscope technique to determine pulse compliance with the mask, it is important that successive traces of the pulses overlay in order to suppress the effects of low frequency jitter. This can be accomplished by several techniques [e.g. a) triggering the oscilloscope on the measured waveform or b) providing both the oscilloscope and the pulse output circuits with the same clock signal].

Note 4 – For the purpose of these masks, the rise time and decay time should be measured between -0.4V and 0.4V , and should not exceed 2ns.

Note 5 – The inverse pulse will have the same characteristics, noting that the timing tolerance at the level of the negative and positive transitions are $\pm 0.1\text{ns}$ and $\pm 0.5\text{ns}$ respectively.

Figure 3 – Mask of a Pulse corresponding to a binary One in STS-3 mode

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER SPECIFICATIONS

The following specifications are met with the external components.

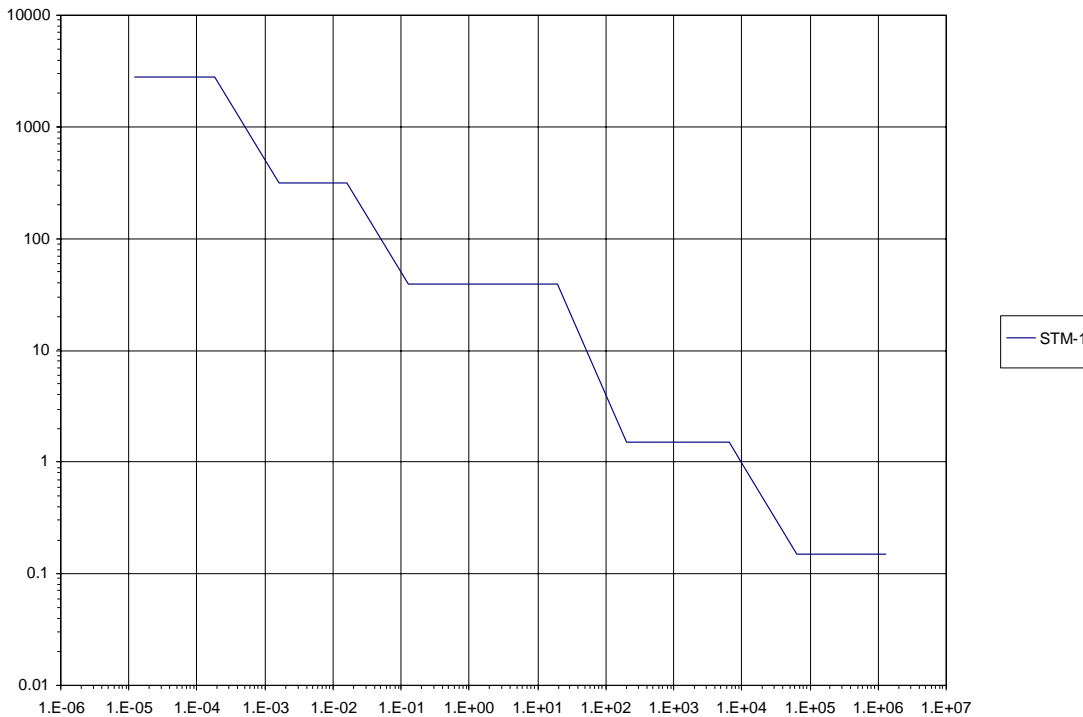
| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---------------|-----------|------|-----|-----|------|
| LOS Threshold | | 0.05 | 0.1 | 0.2 | V |

RECEPTION PERFORMANCE

| | | | | | |
|-------------|----------------|----|--|--|----|
| Return Loss | 7MHz to 240MHz | 15 | | | dB |
|-------------|----------------|----|--|--|----|

RECEIVER JITTER TOLERANCE

STS-3 and OC-3 jitter tolerance specifications are in ANSI T1.105.05-1994 and Telcordia TR-NWT-000253, Issue 2, Dec. 1991. STM-1 specifications are in ITU-T G.825. They are identical except that STM-1 specifies both jitter and wander. The STM-1 specification is the tightest and covers the largest frequency range.



| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|----------------------------------|-------------------|------|-----|-----|------|
| Receiver Jitter Tolerance | 12μHz to 178μHz | 2800 | | | UI |
| | 1.6mHz to 15.6mHz | 311 | | | |
| Note 1: Not tested in production | 125mHz to 19.3 Hz | 39 | | | |
| | 500Hz to 6.5kHz | 1.5 | | | |
| | 65kHz to 3.5MHz | 0.15 | | | |

ELECTRICAL SPECIFICATIONS (continued)

RECEIVER JITTER TRANSFER FUNCTION

The receiver clock recovery loop filter characteristics such that the receiver has the following transfer function. The corner frequency of the PLL is approximately 100 kHz.



| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|-----------------------------------|---------------|-----|-----|-----|---------------|
| Receiver Jitter transfer function | below 100 kHz | | | 0.1 | dB |
| Jitter transfer function roll-off | | | 20 | | dB per decade |
| Note 1: Not tested in production | | | | | |

APPLICATION INFORMATION

EXTERNAL COMPONENTS:

| COMPONENT | PIN(S) | VALUE | UNITS | TOLERANCE |
|--------------------|--------|-------|------------|-----------|
| Reference Resistor | RFO | 31.6 | k Ω | 1% |
| Filter Capacitor | LF1 | 470 | nF | 5% |

TRANSFORMER SPECIFICATIONS:

| COMPONENT | VALUE | UNITS | TOLERANCE |
|-------------|-------|-------|-----------|
| Turns Ratio | | 1:1 | 3% |

Suggested Manufacturer: Halo, MiniCircuits, Belfuse, Tamura

CRYSTAL SPECIFICATIONS:

| COMPONENT | VALUE | UNITS | TOLERANCE |
|--|-------|-------|------------|
| Center Frequency | 19.44 | MHz | +/- 20 ppm |
| Load Capacitor – XTAL1 to ground; XTAL2 to ground <ul style="list-style-type: none"> ➤ Please check datasheet of crystal manufacturer for optimal load capacitor values. | 27 | pF | |

PECL INTERFACE COMPONENTS:

| COMPONENT | VALUE | UNITS | TOLERANCE | |
|----------------------------------|-----------------|----------|-----------|----|
| Output Bias Resistor, R_{BIAS} | $V_{CC} = 5V$ | 250 | Ω | 5% |
| | $V_{CC} = 3.3V$ | 140 | Ω | 5% |
| Termination Resistor, R_{TERM} | 100 | Ω | 5% | |

When the PECL signals travel one inch or less, lower power operation can be achieved by increasing R_{BIAS} and eliminating R_{TERM} .

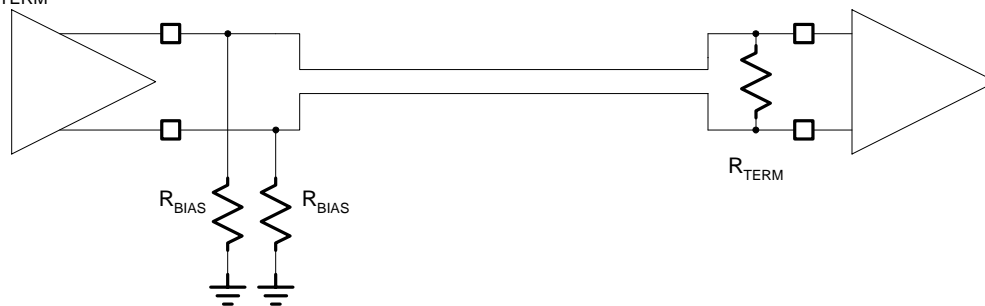
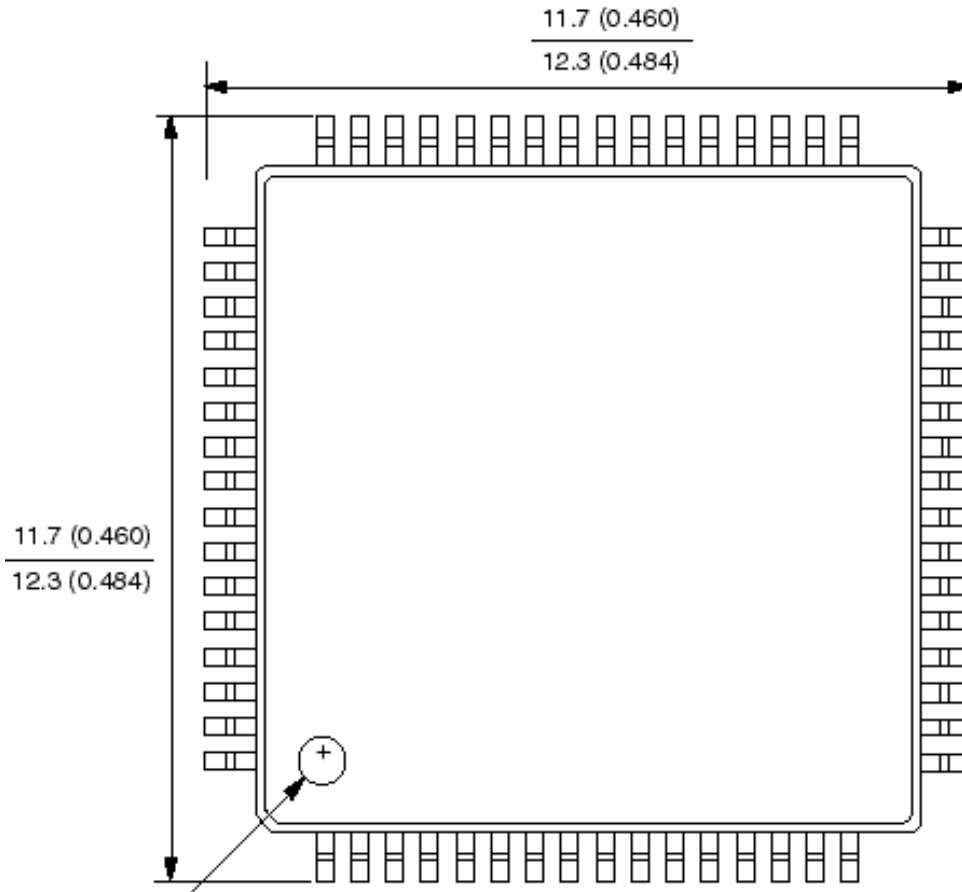
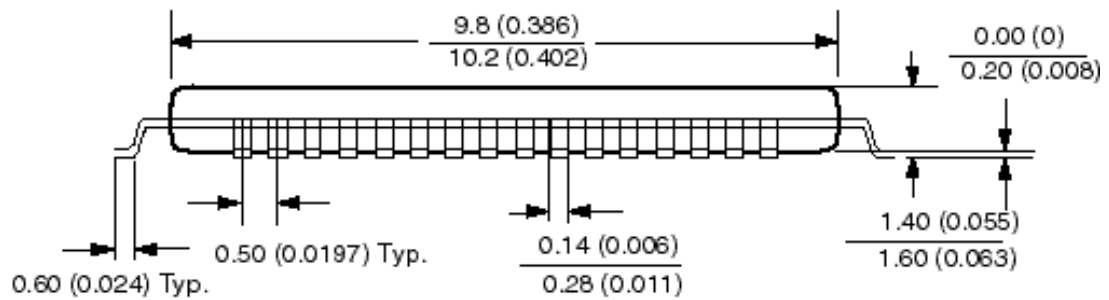


FIGURE 4. PECL INTERFACE

MECHANICAL SPECIFICATIONS



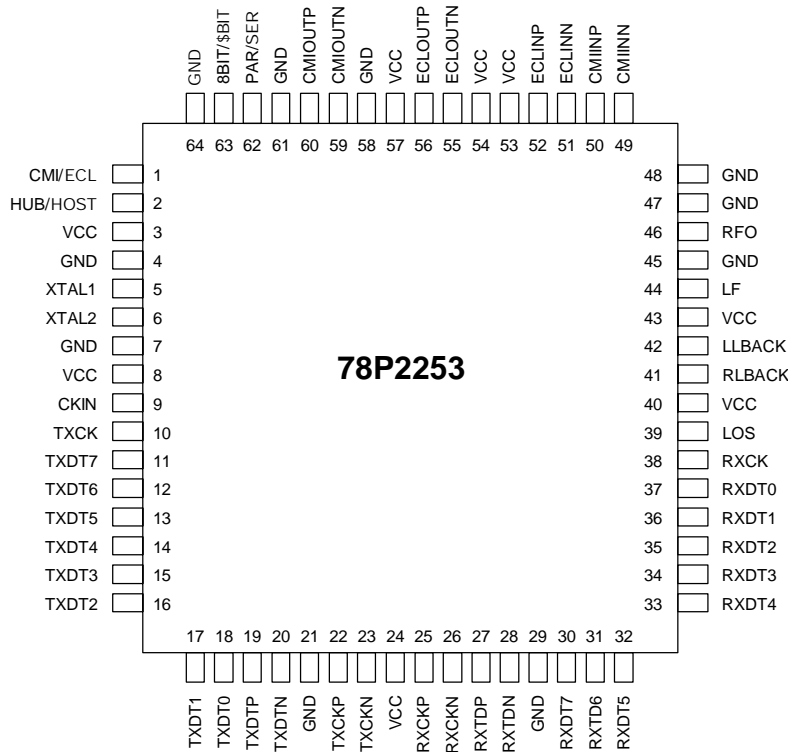
PIN No. 1 Indicator



64-TQFP (JEDEC LQFP)
Mechanical Specification

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Pin TQFP (JEDEC LQFP)
78P2253-IGT

ORDERING INFORMATION

| PART DESCRIPTION | ORDER NUMBER | PACKAGE MARK |
|---------------------------------------|---------------|------------------------|
| 78P2253 64-pin Plastic LQFP | 78P2253-IGT | 78P2253-IGT xxxxxx |
| 78P2253 64-pin Plastic LQFP-Lead Free | 78P2253-IGT/F | 78P2253-IGT xxxxxxF |

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